



Agenda

- Memory cell
- Fabrication process
- Device organization
- Write operation
- Read operation
- Bit area comparison
- Summary

Fig. 1

Memory Cell (1/3)

- Two-terminal cell contains a diode and antifuse.
- Wordlines and bitlines are shared between layers.

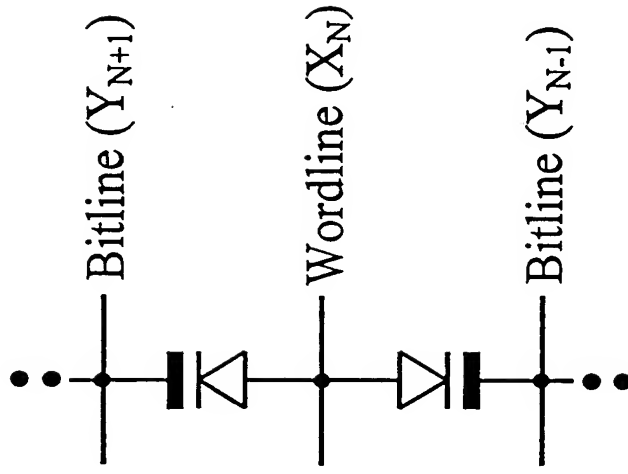
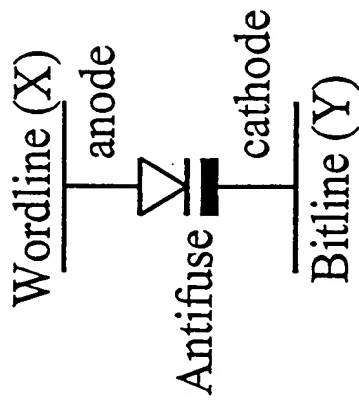


Fig. 2

Memory Cell (2/3)

- Cells built from polycrystalline silicon.
- Stacked for maximum density.

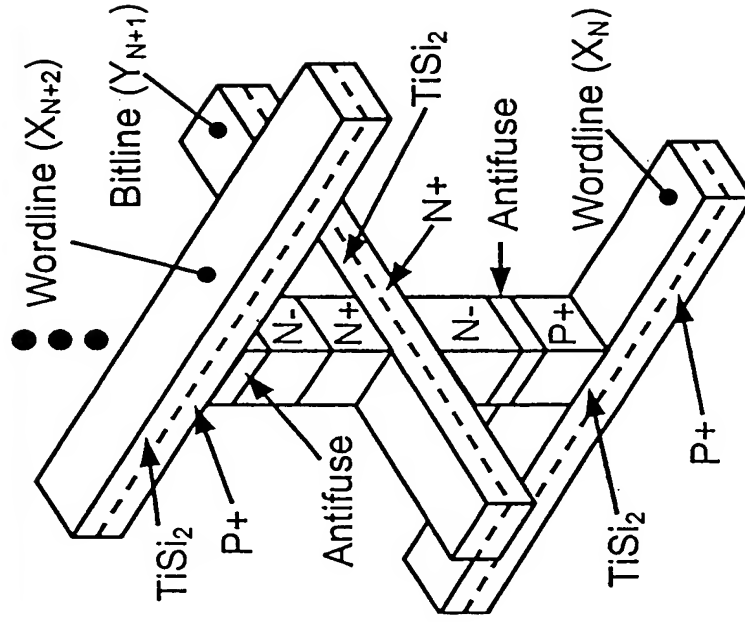


Fig. 3

Memory Cell (3/3)

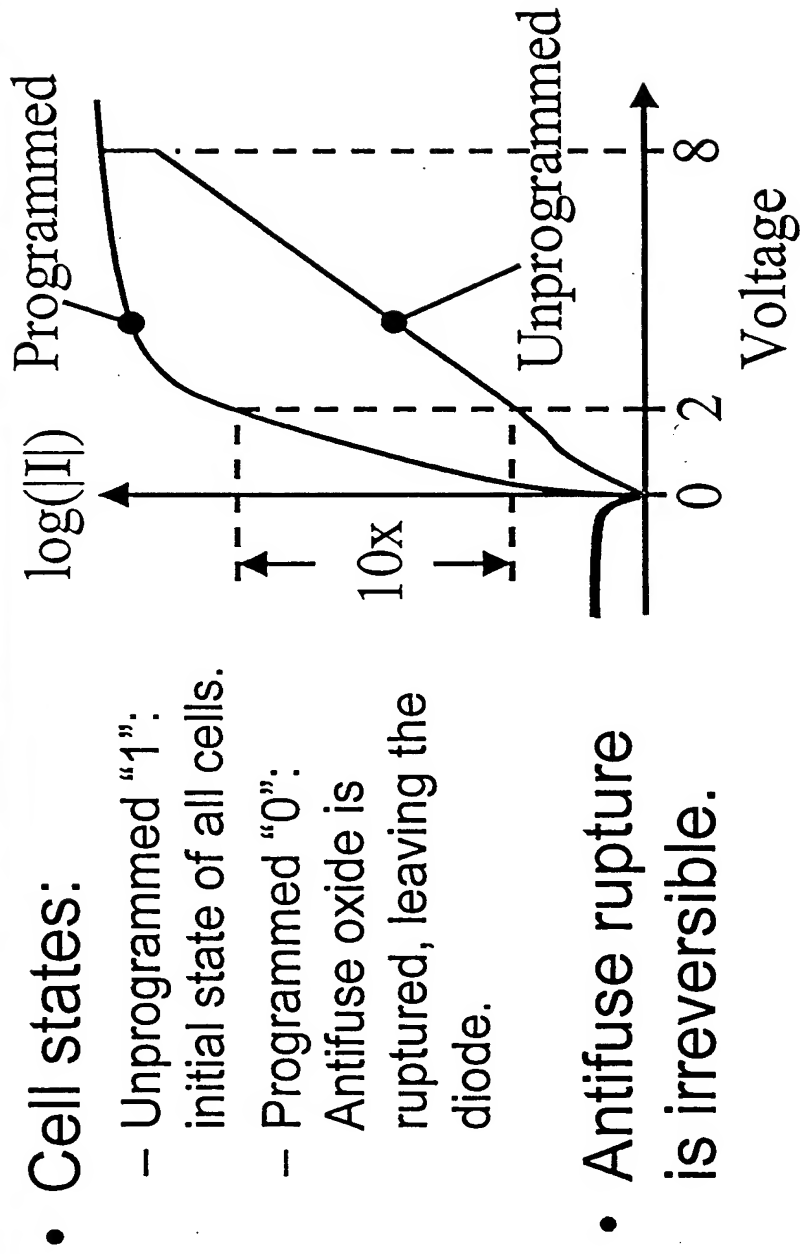


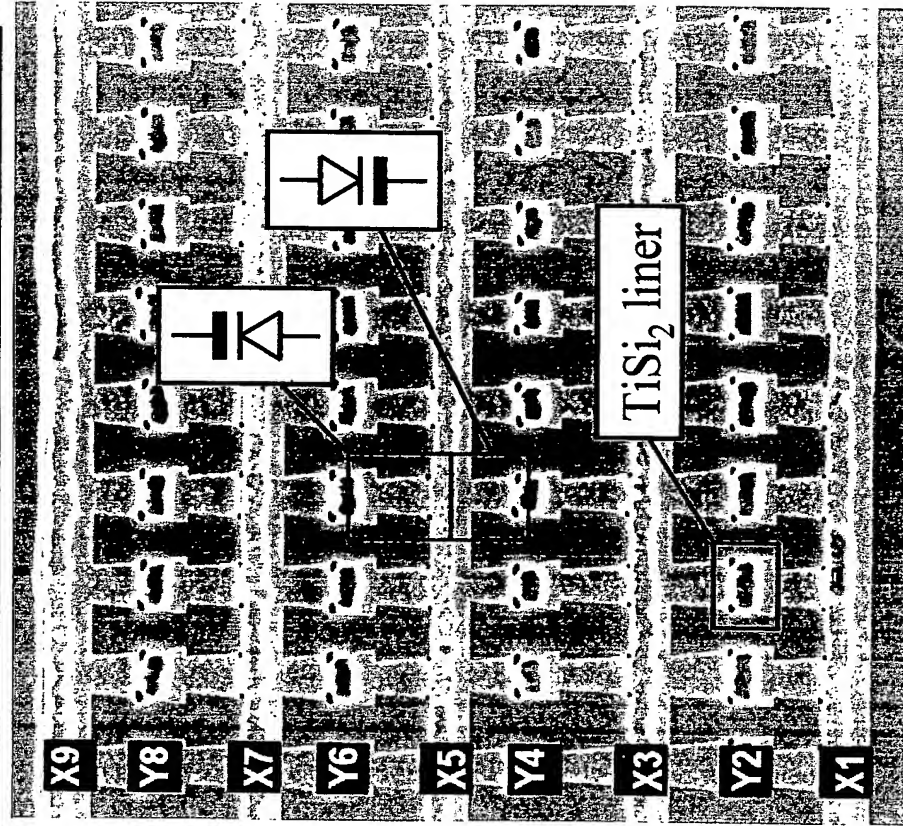
Fig. 4

Process Highlights

- 0.25 μ m Nwell CMOS:
 - Single 17.5nm gate oxide;
 - 2 tungsten layers (“R1” and “R2”) for transistor interconnect.
- 8-high stack of memory cells:
 - 5 wordline layers, 4 bitline layers;
 - Cell is 0.50 μ m x 0.50 μ m x (1/8);
 - Vias from array to CMOS.
- 1 Al layer for bond pads, global signals and power distribution.

Fig. 5

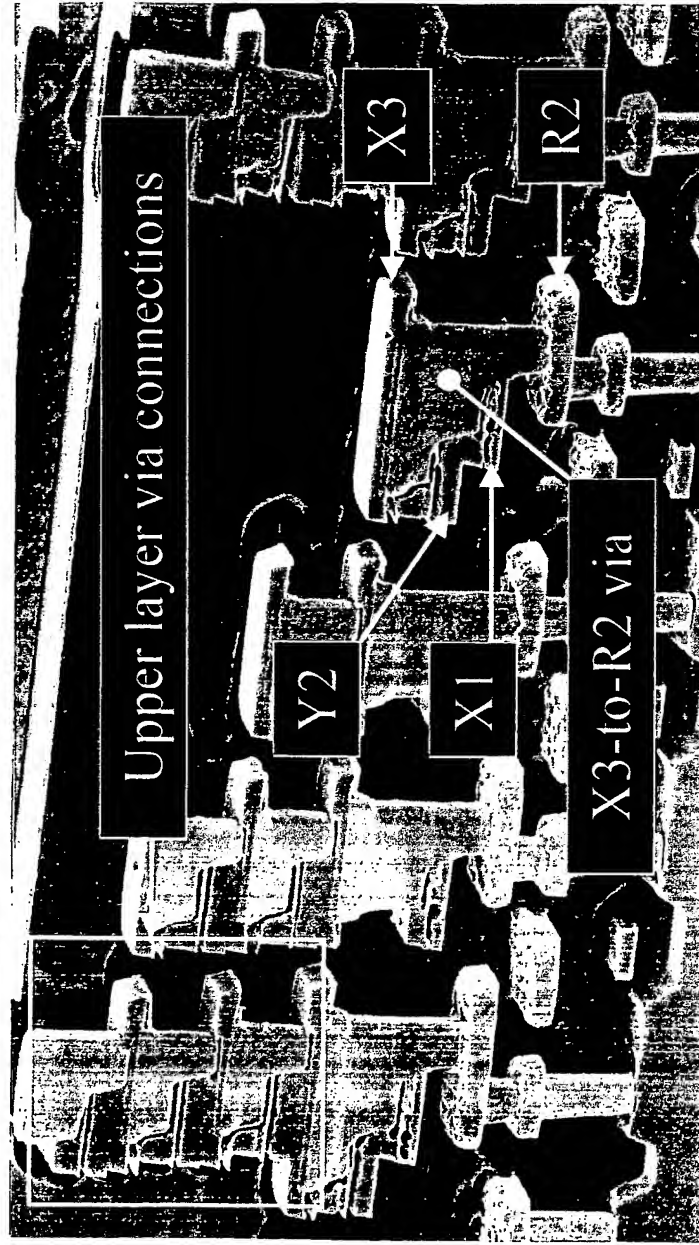
Array of Stacked Memory Cells



- Wordlines:
X{1, 3, 5, 7, 9}.
- Bitlines:
Y{2, 4, 6, 8}.
- (8+1) wiring levels give (8) layers of cells.
- TiSi₂ liners reduce sheet rho (2-3 Ω/\square).

Fig. 6

Connections to the Array



- Vertical interconnects span 3 memory layers; 4 via masks service 9 layers.

Fig. 7

Tile Organization

- Cells built in 1MB sub-arrays (“Tiles”):
 - 1024 wordlines x 1024 bitlines x 8 layers;
 - Additional wordlines and bitlines for test and repair.
- Row and column decoders, bias circuits, and sense amplifiers laid out beneath the 1MB Tiles.
- $2+\epsilon$ transistors per memory line, where ϵ is the amortized cost of the decoders and bias circuits.

Fig. 8

Die Organization (1/3)

- 1MB Tiles organized in a “Checkerboard” pattern.
- Checkerboard design maximizes row and column decoder sharing.
- 1MB Tile size chosen for optimum power / BW / programmability / density.

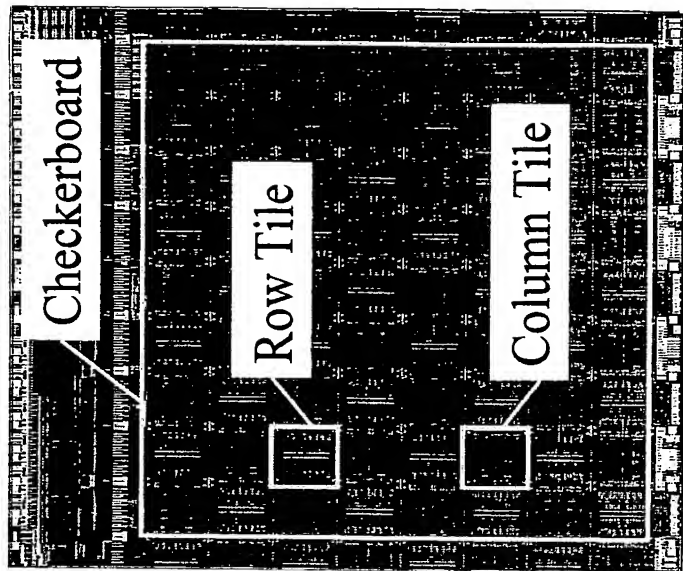


Fig. 9

Die Organization (2/3)

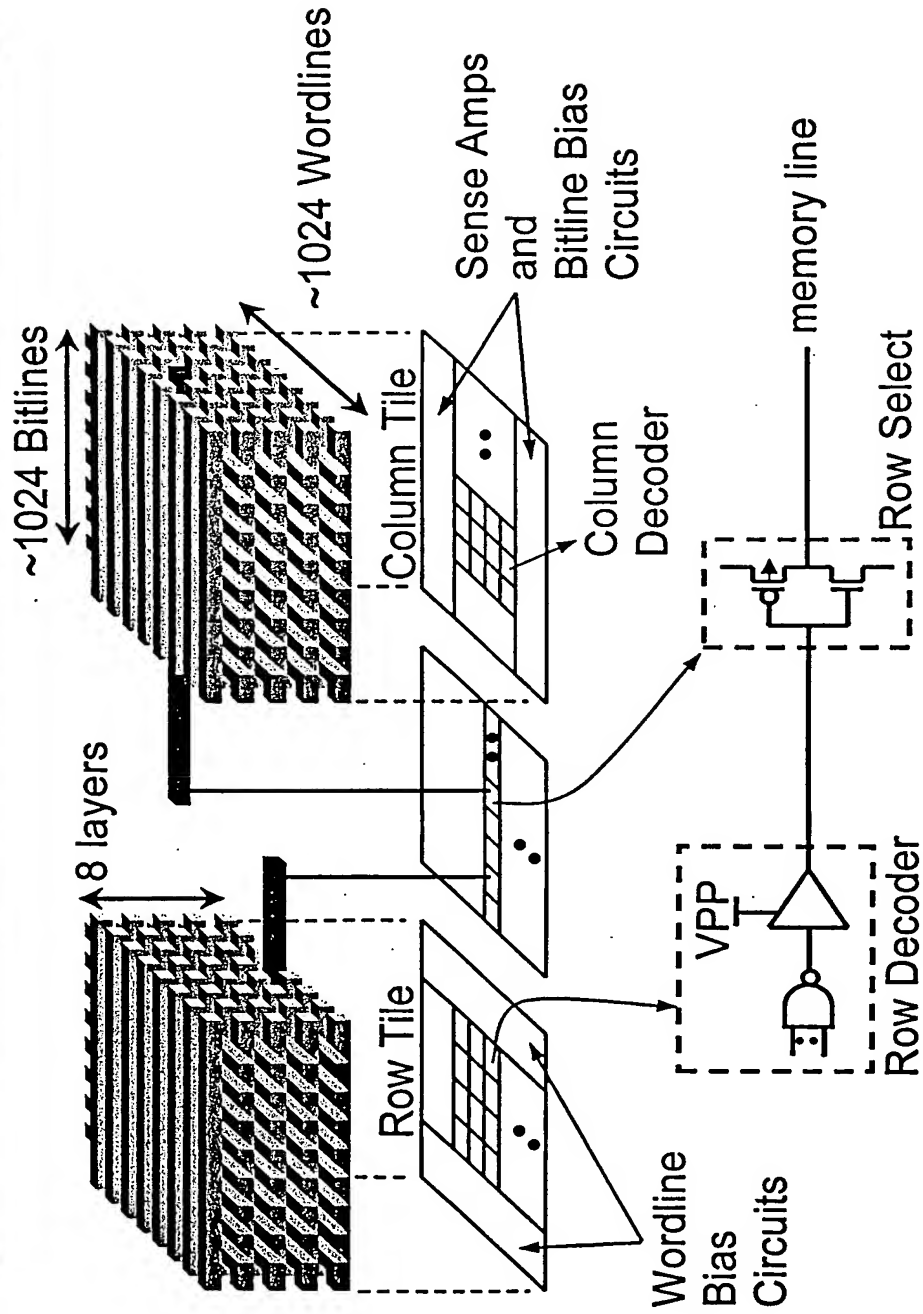


Fig. 10

Die Organization (3/3)

- Chip contains 8 horizontal Stripes, with 9 Tiles/Stripe.
- User pages are distributed among 8 Tiles in a Stripe.
- 9th Tile in each Stripe is dedicated to ECC.

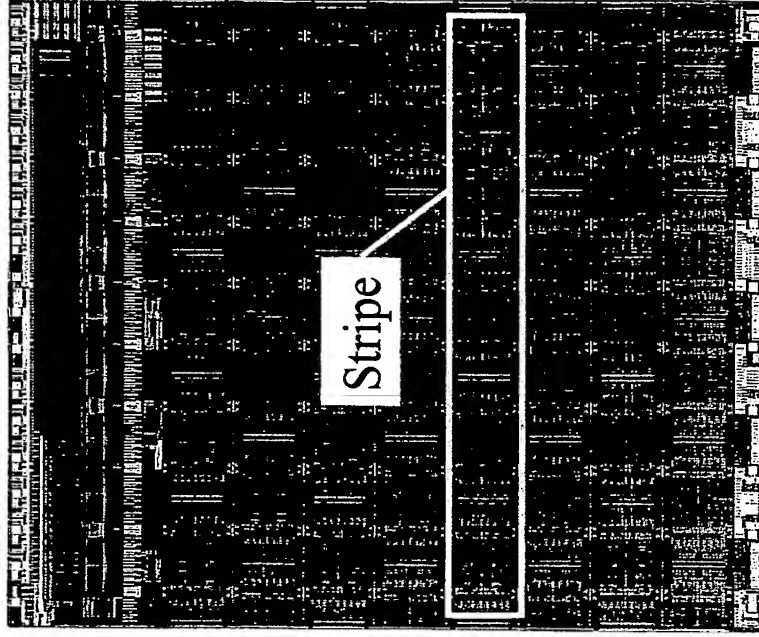


Fig. 11

Fault Tolerance

- Single-bit correction, double-bit detection ECC included on the die:
 - (72,64) Hamming code protection on each 64-bit “octbyte”;
 - 8 additional syndrome bits per 64 user bits;
 - ECC is performed 100% on-chip; external system is unaware of ECC operations.
- Flexible row repair allows factory or on-the-fly (field) replacement.

Fig. 12

Chip Block Diagram

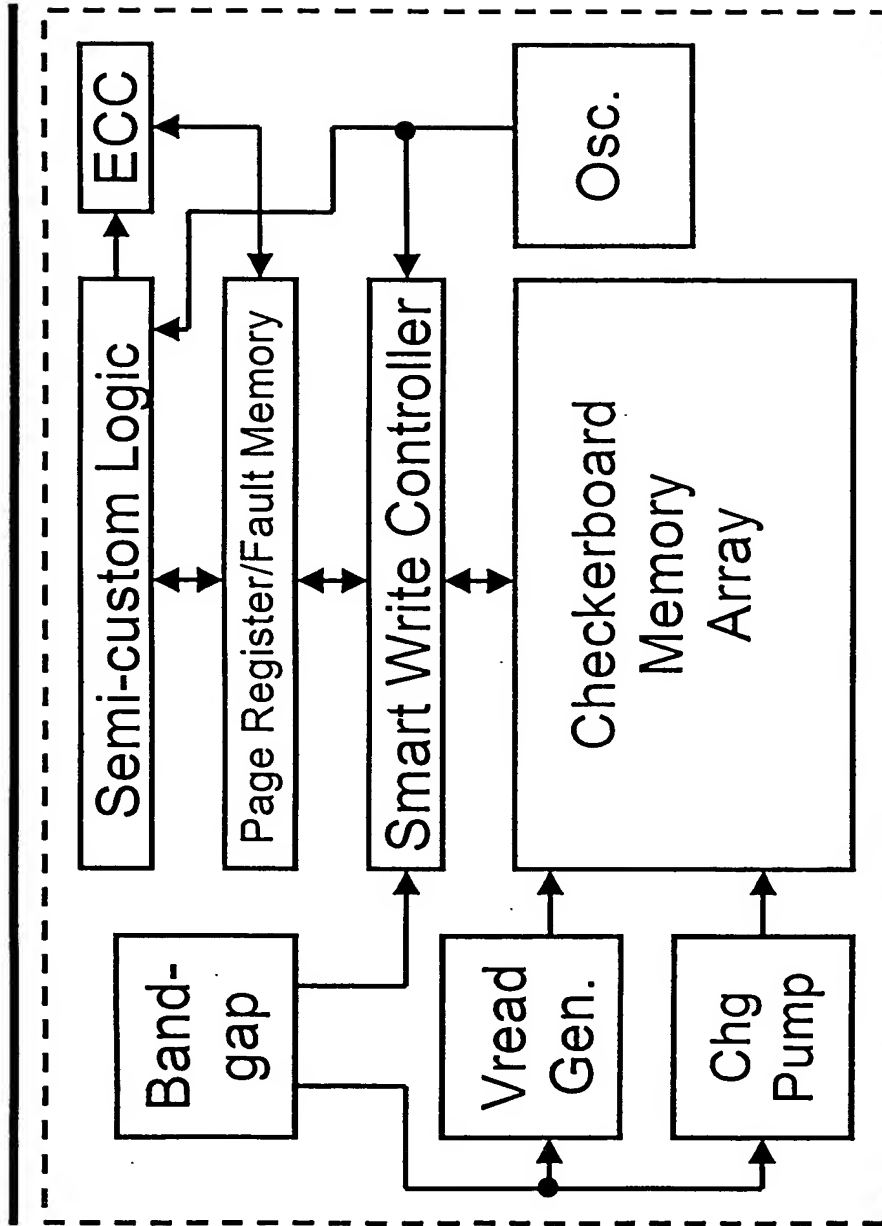


Fig. 13

Write Operation (1/2)

- Write: Wordline=9V, Bitline=0V.

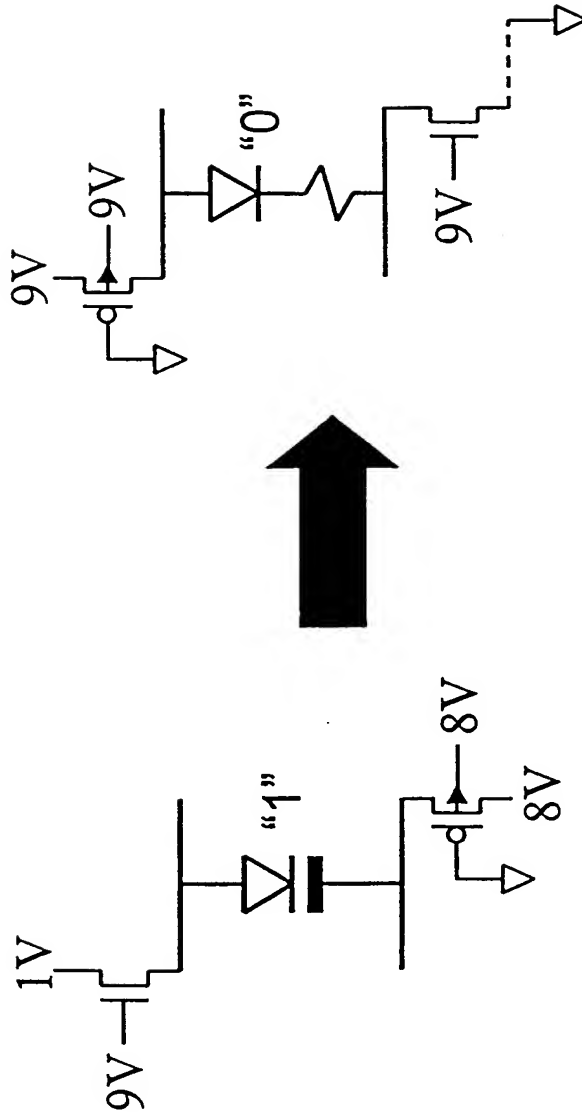


Fig. 14

Write Operation (2/2)

- Smart Write block:
 - Skips over “1” bits;
 - Uses the read sense amp to dynamically detect when an antifuse ruptures;
 - Immediately proceeds to the next bit, accelerating writes.
 - Detects programming fails.
- More than one fail in an ECC word (8B data + 1B ECC) initiates reprogramming to a redundant page location.

Fig. 15

Read Operation

- Wordline = $2.4V$ = “Vread”.
- Bitline = Dummy bitline = $0.4V$:
 - Dummy bitline provides common mode cancellation of array noise.
- Current-mode sensing:
 - Active mirror clamps memory cell voltage to $2.0V$, cell current is compared to IREF.
- 72 sense amps active simultaneously:
 - All 9 Tiles in a Stripe are active;
 - Memory cells above Row Tiles are read with sense amps located in adjacent Stripes.

Fig. 16

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Sensing IREAD=300nA

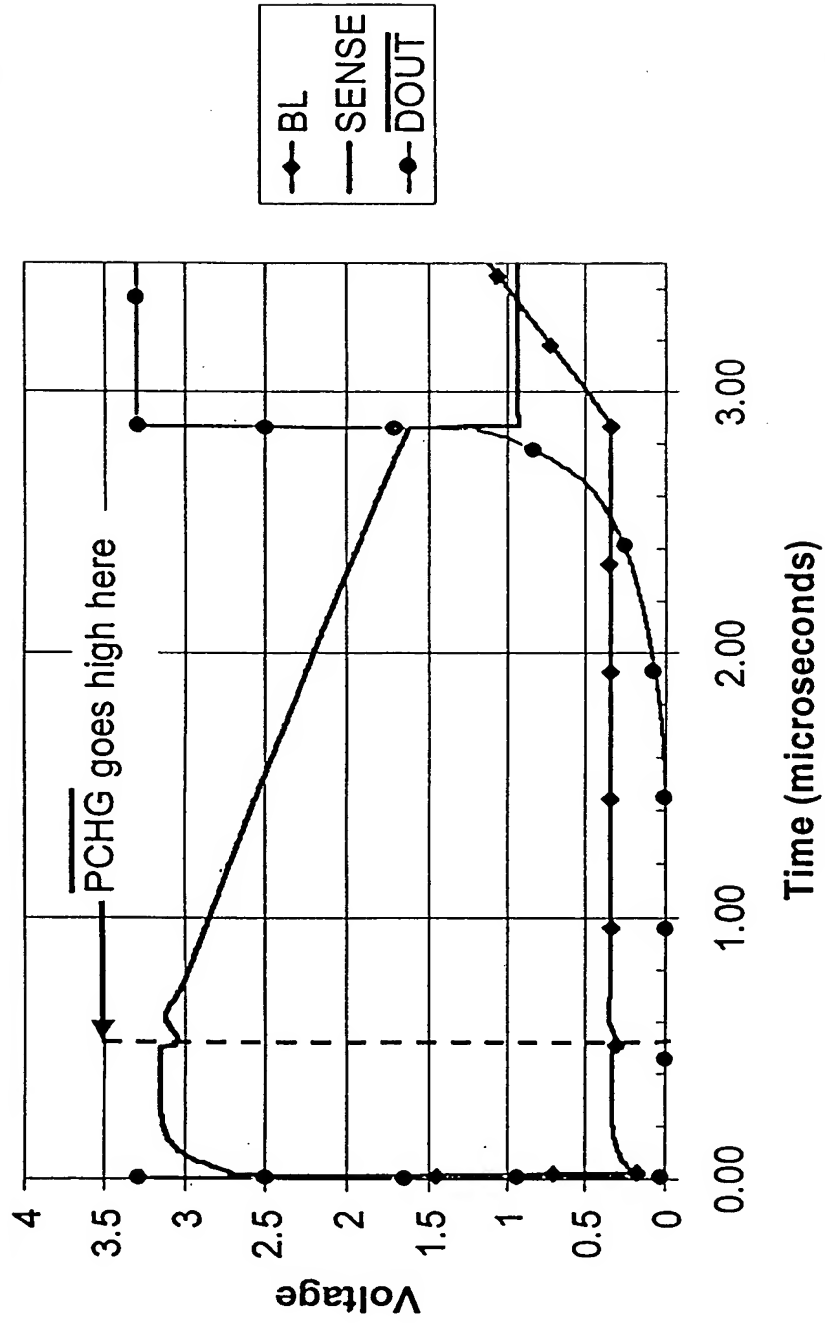


Fig. 18

Vread Generator

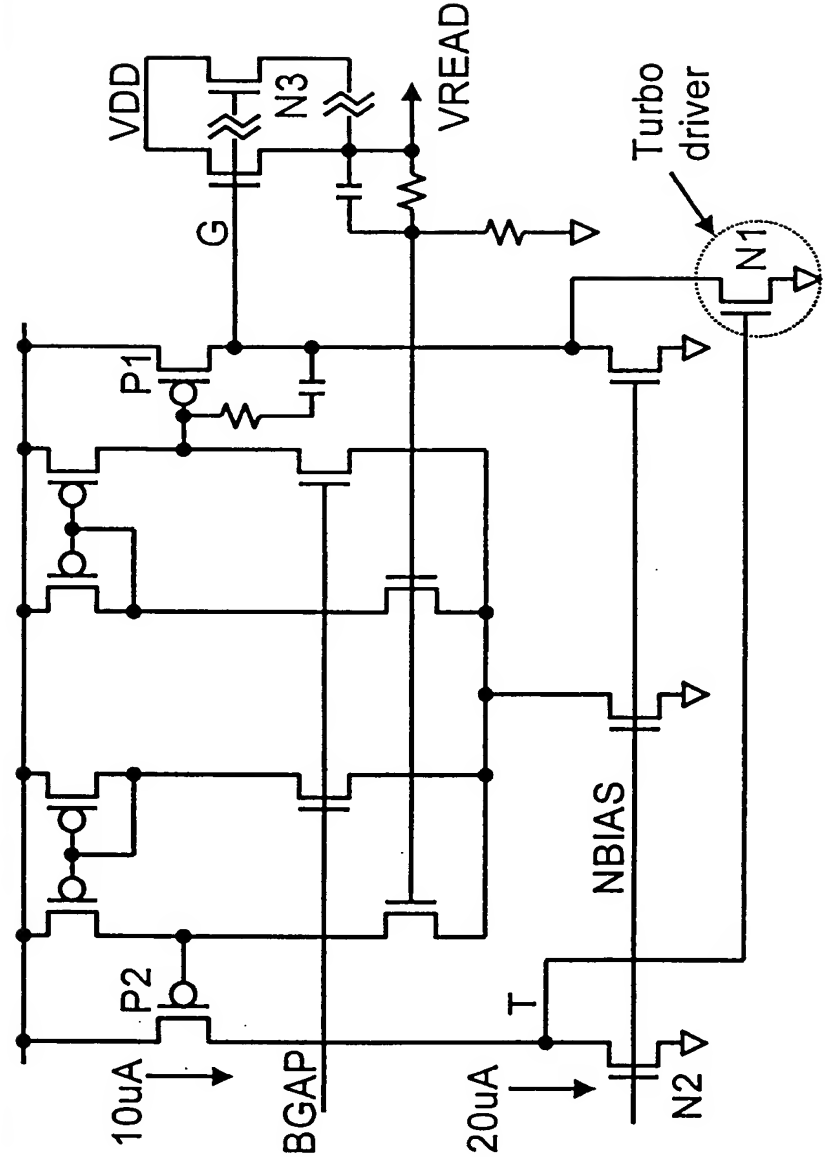


Fig. 19

Vread Generator

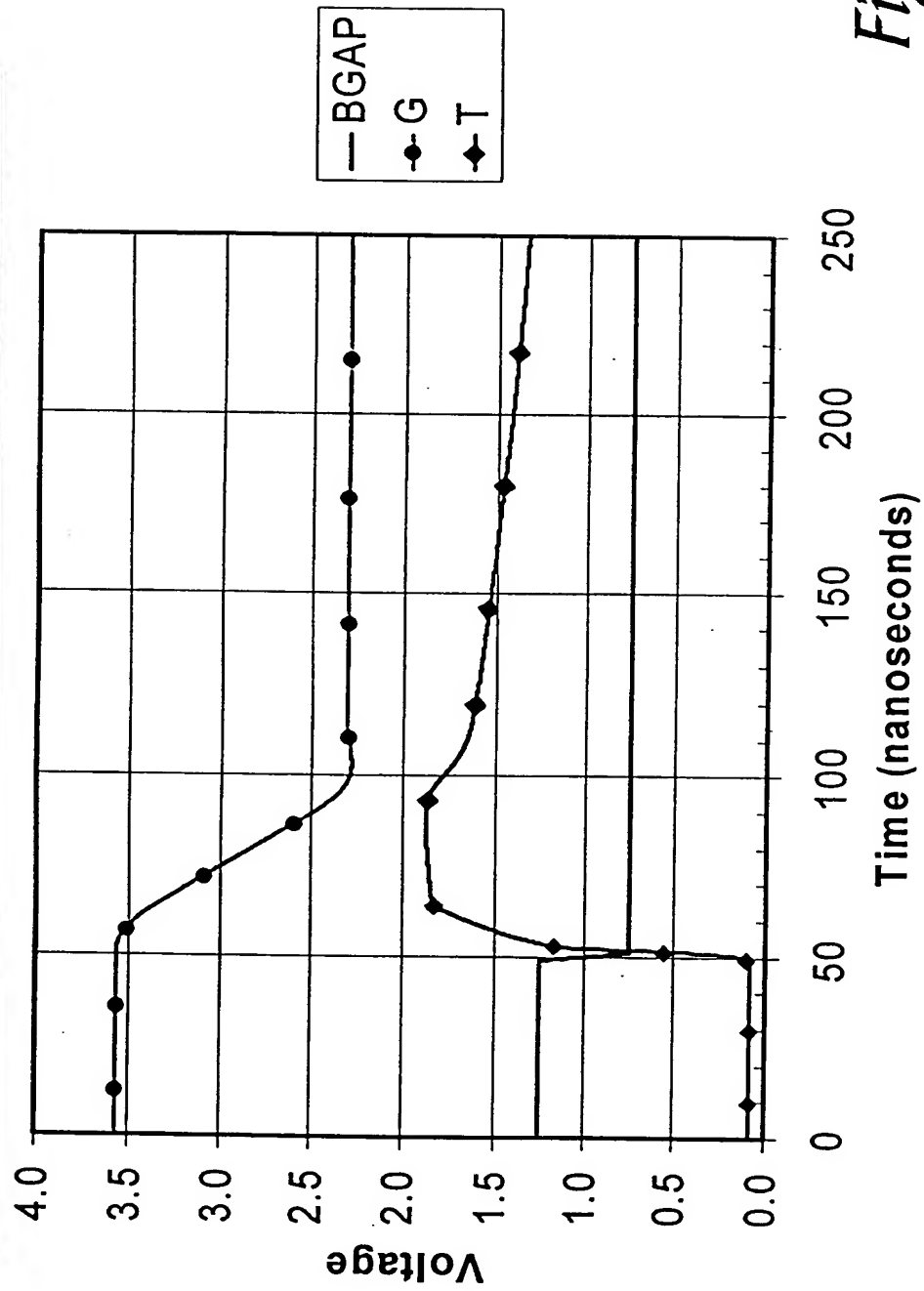


Fig. 20

Bit Area Comparison

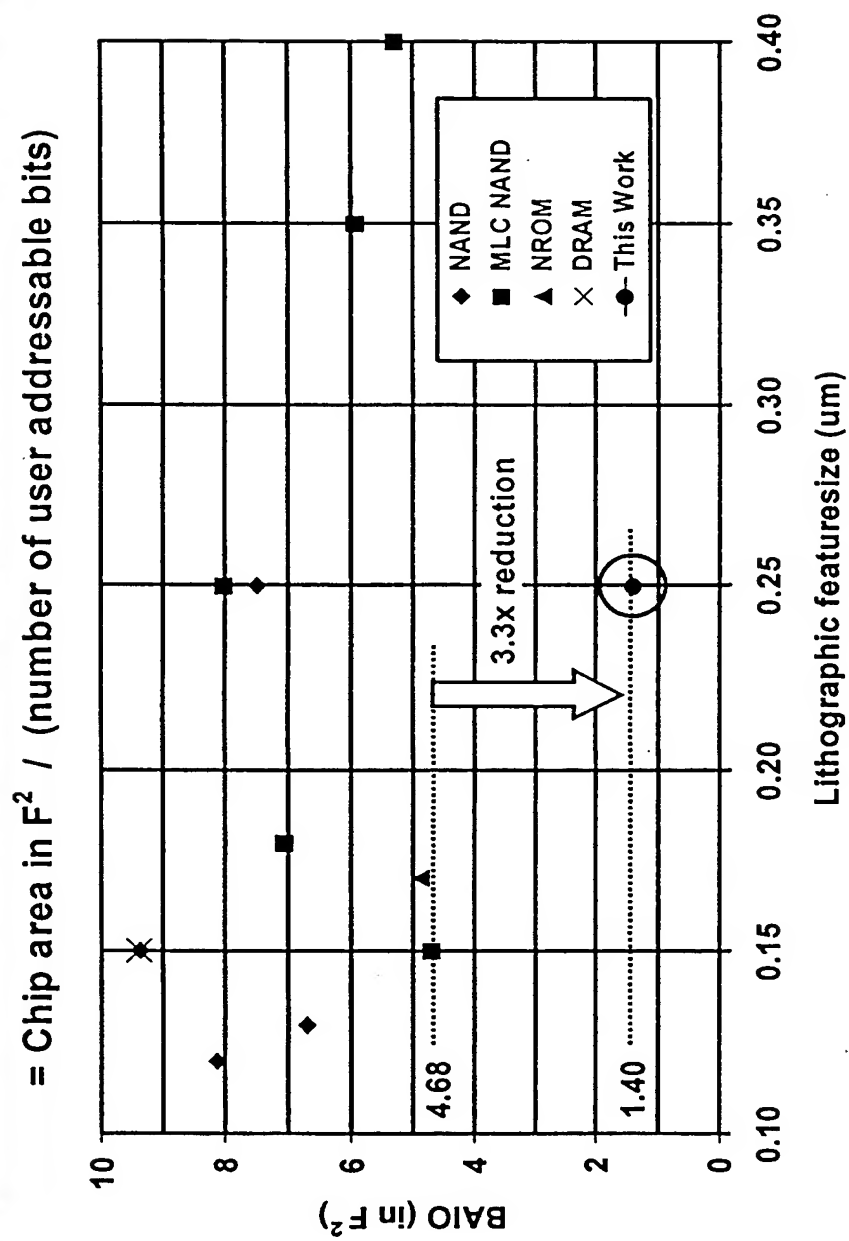


Fig. 21

Device Characteristics

Technology	0.25um CMOS, Tox = 17.5nm
Cell type	OTP, diode+antifuse, 0 transistors
Cell size	0.50um X 0.50um
Chip size	6.7mm X 7.2mm = 48.3mm ²
Wiring	2 layers W + 1 layer Al
Power	VDD = 2.7 – 3.6V IDD = 30mA
Bandwidth	1.0 MB/s read, 0.5 MB/s write
Organization	128K pages X (512 + 16) bytes/page
Fault tolerance	(72,64) modified Hamming ECC
Application	Digital media, handhelds, file storage

Fig. 22

Summary

- 3-dimensional memory array with cells vertically stacked 8-high.
- Two terminal, antifuse/diode memory cell built in polysilicon.
- 512 Mbit PROM, generic NAND Flash interface.
- SEC-DED ECC included on-die.
- 3.3x more bits per F² than MLC NAND Flash.

Fig. 23